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EPSON

Universal Interface-compatible
For TM Series Printers
Parallel Universal Board for IEEE 1284 Interface

UB-P02II

Specification

STANDARD	
Rev. No.	B
Notes	

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SEIKO EPSON CORPORATION

MATSUMOTO MINAMI PLANT
2070 KOTOBUKI KOAKA, MATSUMOTO-SHI, NAGANO, 399-8702 JAPAN
PHONE(0263)86-5353 FAX(0263)86-9923

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REVISION SHEET

The table below indicates which pages in this specification have been revised.
Before reading this specification, be sure you have the correct version of each page.

Revisions		Design Section			Sheet Rev. No.					
Rev.	Document	WRT	CHK	APL	Sheet	Rev.	Sheet	Rev.	Sheet	Rev.
A	Enactment				I	A				
B	Change	Watanabe	-	Yamaji	II	A				
					1	A				
					2	A				
					3	B				
					4	A				
					5	A				
					6	A				
					7	A				
					8	B				
					9	B				

TITLE	Front Part					Contents	Appendix	Total
UB-P02II Specification (STANDARD)	Cover	Rev. Sheet	Scope	General Description	Table of Contents			
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REVISION SHEET

REV.	SHEET	CHANGED CONTENTS
A	All	Newly enacted.
B	3 8 9	Table 2.3.1: Pin number 34 was changed from DK_STATUS to NC. Figure 3.2.1: External View was changed. 4. EMC APPLIED: The content of the description was changed to the latest standard.

TITLE

UB-P02II
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EPSON	TITLE **UB-P02II** Specification (STANDARD)	SHEET REVISION A	NO.	
			NEXT II	SHEET I

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Table of Contents

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1. GENERAL DESCRIPTION

1.1 Overview

The UB-P02Ⅱ is installed in the TM series printer and is a parallel interface board (IEEE 1284 (*1) compatible) which can communicate with the host PC.

*1: Copyright ©1994 by the Institute of Electrical and Electronic Engineers, Inc.

1.2 Printers in which the UB-P02Ⅱ can be installed

The UB-P02Ⅱ can be installed in all TM series printers which support the UIB (universal interface board).

NOTE: If the TM printer is equipped with the UB-P02Ⅱ, the DM-D connector on the TM series printer cannot be used.

2. ELECTRICAL SPECIFICATIONS

2.1 Communications Specifications

Data transfer format:	8-bit parallel
Synchronization method:	Synchronized with externally supplied nStrobe signal
Flow control:	According to nAck signal and Busy signal
Signal levels:	TTL-compatible
Connector:	57RE-40360-830B (DDK) or equivalent (1284 Type B)

Reverse communications (TM Series printer -> Host computer):
Nibble and Byte mode

2.2 Reverse Mode (Printer -> Host Communications)

Either nibble mode or byte mode is used to transfer status data from a TM Series printer equipped with a 1284 interface board to the host computer.

Nibble/byte mode transfers are defined for asynchronous transfers of data controlled by the host computer from the TM Series printer to the host computer.

In a nibble mode data transfer, existing control lines are used to transfer data four bits (a "nibble") at a time. In byte mode, the eight data lines (bits) are used for bi-directional transfer. In either case, simultaneous execution with compatibility mode is not possible; in such a case, half-duplex communications result.

Note that the 1284 nibble/byte modes are subject to change without notice.

2.3 Interface Connector Pin Assignments in Each Mode

Table 2.3.1 Table of TM Series Printer Interface Connector Pin Assignments

Pin	Source	Compatibility Mode	Nibble Mode	Byte Mode
1	Host	nStrobe	HostClk	HostClk
2	Host/Ptr	Data0(LSB)	Data0(LSB)	Data0(LSB)
3	Host/Ptr	Data1	Data1	Data1
4	Host/Ptr	Data2	Data2	Data2
5	Host/Ptr	Data3	Data3	Data3
6	Host/Ptr	Data4	Data4	Data4
7	Host/Ptr	Data5	Data5	Data5
8	Host/Ptr	Data6	Data6	Data6
9	Host/Ptr	Data7(MSB)	Data7(MSB)	Data7(MSB)
10	Printer	nAck	PtrClk	PtrClk
11	Printer	Busy	PtrBusy/Data3,7	PtrBusy
12	Printer	Perror	AckDataReq/Data2,6	AckDataReq
13	Printer	Select	Xflag/Data1,5	Xflag
14	Host	nAutoFd	HostBusy	HostBusy
15		NC	ND	ND
16		GND	GND	GND
17		FG	FG	FG
18	Printer	Logic-H	Logic-H	Logic-H
19		GND	GND	GND
20		GND	GND	GND
21		GND	GND	GND
22		GND	GND	GND
23		GND	GND	GND
24		GND	GND	GND
25		GND	GND	GND
26		GND	GND	GND
27		GND	GND	GND
28		GND	GND	GND
29		GND	GND	GND
30		GND	GND	GND
31	Host	nInit	nInit	nInit
32	Printer	nFault	nDataAvail/Data0,4	nDataAvail
33		GND	ND	ND
34		NC	ND	ND
35	Printer	+5V	ND	ND
36	Host	nSelectIn	1284-Active	1284-Active

NOTES: 1) A signal name that begins with "n" is an active low signal. If the host computer lacks even one of the above signal lines, bi-directional communications are not possible.

2) Each signal line in the interface must be implemented using a twisted pair wire, and the return side must be connected to the signal ground level.

3) The interface requirements all use TTL level as a reference point, and must satisfy the characteristics shown in Section 2.4. The rise and fall time of each signal should be 0.5 µs or less.

4) Do not ignore a nAck signal or a Busy signal and attempt to transfer data. If either type of signal is ignored, the data will be lost. (Data transfers to the printer must either check the nAck signal or must be performed when the Busy signal is low.)

5) The interface cable must be as short as possible.

* NC: Not connected ND: Not defined

2.4 Electrical Characteristics

Table 2.4.1 DC Characteristics (Except for logic-H and +5V signals)

Characteristic	Symbol	Prescribed value		Conditions
		Min	Max	
Output high voltage	V_{OH}	*2.4 V	5.5 V	*I_{OH} = 0.32 mA
Output low voltage	V_{OL}	-0.5 V	*0.4 V	*I_{OL} = -12 mA
Output high current	I_{OH}	0.32 mA	-	V_{OH} = 2.4 V
Output low current	I_{OL}	-12 mA	-	V_{OL} = 0.4 V
Input high voltage	V_{IH}	20 V	-	
Input low voltage	V_{IL}	-	0.8 V	
Input high current	I_{IH}	-	-0.32 mA	V_{IH} = 2.0 V
Input low current	I_{IL}	-	12 mA	V_{IL} = 0.8 V

Table 2-4-1 Logic-H Signal Transmitting Side Characteristics

Characteristic	Symbol	Prescribed value		Conditions
		Min	Max	
Output high voltage	V_{OH}	3.0 V	5.5 V	
Output low voltage	V_{OL}	-	2.0 V	Power off

Table 2-4-2 +5V Signal Transmitting Side Characteristics

Characteristic	Symbol	Prescribed value		Conditions
		Min	Max	
Output high voltage	V_{OH}	*2.4 V	5.5 V	*I_{OH} = 0.32 mA
Output low voltage	V_{OL}	-	- **	Power off
Output high current	I_{OH}	-	0.32 mA	V_{OH} = 2.4 V
Output low current	I_{OL}	- **	-	Power off

**When the power is off, V_{OL} and I_{OL} are not guaranteed.

2.5 Data Receive Timing (Compatibility Mode)

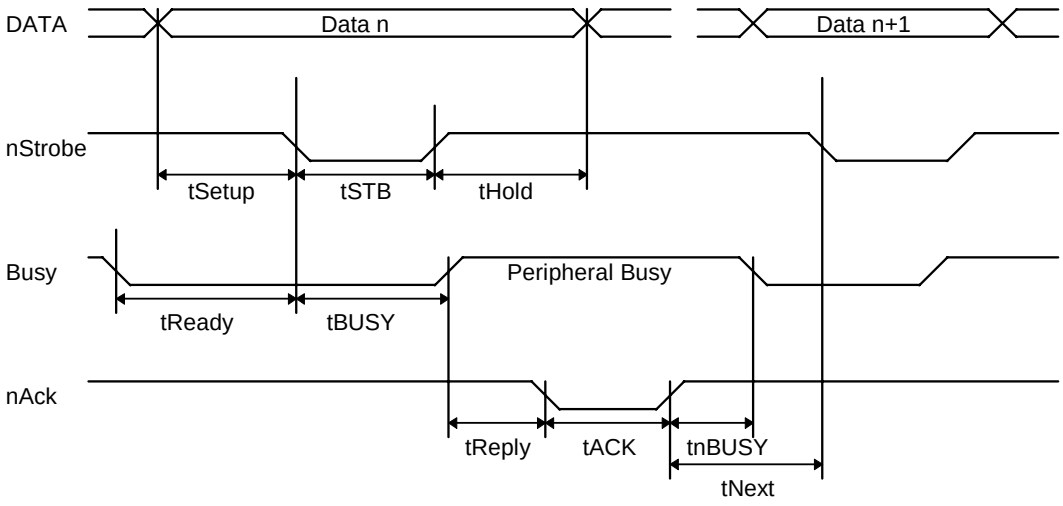


Figure 2.4.1 Compatibility Mode Timing

Table 2.4.4 List of Prescribed Timing Values for Figure 2.4.1

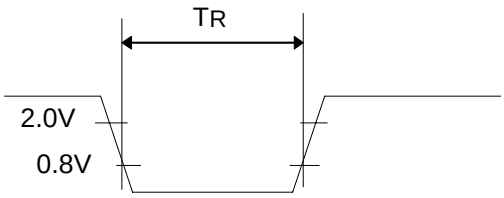
Characteristics	Symbol	Specifications	
		Minimum [ns]	Maximum [ns]
Data Hold Time (host)	tHold-1	750	--
Data Setup Time	tSetup	750	--
STROBE Pulse Width	tSTB	750	--
READY Cycle Idle Time	tReady	0	--
BUSY Output Delay Time	tBUSY	0	500
Data Processing Time	tReply	0	∞
ACKNLG Pulse Width	tACK	500	10 µs
BUSY Release Time	tnBUSY	0	∞
ACK Cycle Idle Time	tNext	0	--

*The printer latches data at the nStrobe falling edge.

2.6 Notes on Using an Interface Signal to Reset the Printer

With this interface board, by setting a DIP switch on the TM Series printer, it is possible to use the nInit signal (pin 31) of the 1284 interface to reset the printer.

To reset the printer the DIP switch or the memory switch of the TM series printer must be set so that the reset signal of #31 pin is enabled. For details on the DIP switches or the memory switches on the TM series printers, refer to the TM series printer specifications.



*Minimum reset pulse width TR: 50 µs (min.)

Figure 2.6.1 Reset Signal Timing

2.7 Receiving Status Information from the Printer through the Bi-directional Parallel Interface

It is possible to send information on the status of the TM Series printer to the host computer by using the bi-directional communications function in IEEE 1284 nibble/byte mode when using the bi-directional parallel interface board.

When an IBM-PC/AT or a compatible system is used as the host computer, it is not possible to send a data receive interrupt to the MPU when using a parallel interface, unlike the case when an RS-232 serial interface is used. Therefore, the following points must be noted.

1) The printer's internal transmission buffer is 99 bytes. Any status information (excluding ASB status information) in excess of 99 bytes is lost. In order to avoid losing any of the status data that is to be sent, it is necessary to establish the receive state (reverse mode) in the host computer side.

   * ASB: Automatic Status Back
     This function reports changes in the status of the TM Series printer. For details, refer to the TM Series printer specifications.

2) When using ASB, it is best to use the waiting-for-receive state (reverse idle mode) as the normal mode for the host computer. If reverse idle mode cannot be used as the normal mode, then it is best to constantly look for data by setting the host computer side to reverse mode at suitable, regular intervals.

3) When using ASB, the ASB status is given priority ahead of other status information in reverse mode. In addition, any ASB status information that is accumulated between the last time the ASB status information was sent and when the newest ASB status information is sent is grouped into a single batch of ASB status information (indicating that there were changes) and is then sent, followed by the newest ASB status information.

Example: The ASB status in the normal (standby) state is as follows:

Status 1	Status 2	Status 3	Status 4
0001 0000	0000 0000	0110 0000	0000 1111

In this state, if near end, cover open, and then cover closed is detected, the following data is accumulated:

	Status 1	Status 2	Status 3	Status 4	
(1)	0001 0000	0000 0000	0110 0011	0000 1111	Near end detection
(2)	0011 1000	0000 0000	0110 0011	0000 1111	Cover open
(3)	0001 0000	0000 0000	0110 0011	0000 1111	Cover closed

The ASB status is then received. The ASB status information that is actually sent is as follows (1 + 2 + 3):

ASB ((1)+(2)+(3))

Status 1	Status 2	Status 3	Status 4
0011 1000	0000 0000	0110 0011	0000 1111

+

and then the final ASB (3):

Status 1	Status 2	Status 3	Status 4
0001 0000	0000 0000	0110 0011	0000 1111

for a total of eight bytes sent.

3. MECHANICAL SPECIFICATIONS

3.1 Overall Dimensions

Approximately 88 mm(W) × 58 mm(D) × 27 mm(H)
(Maximum size containing the plate and the connectors)

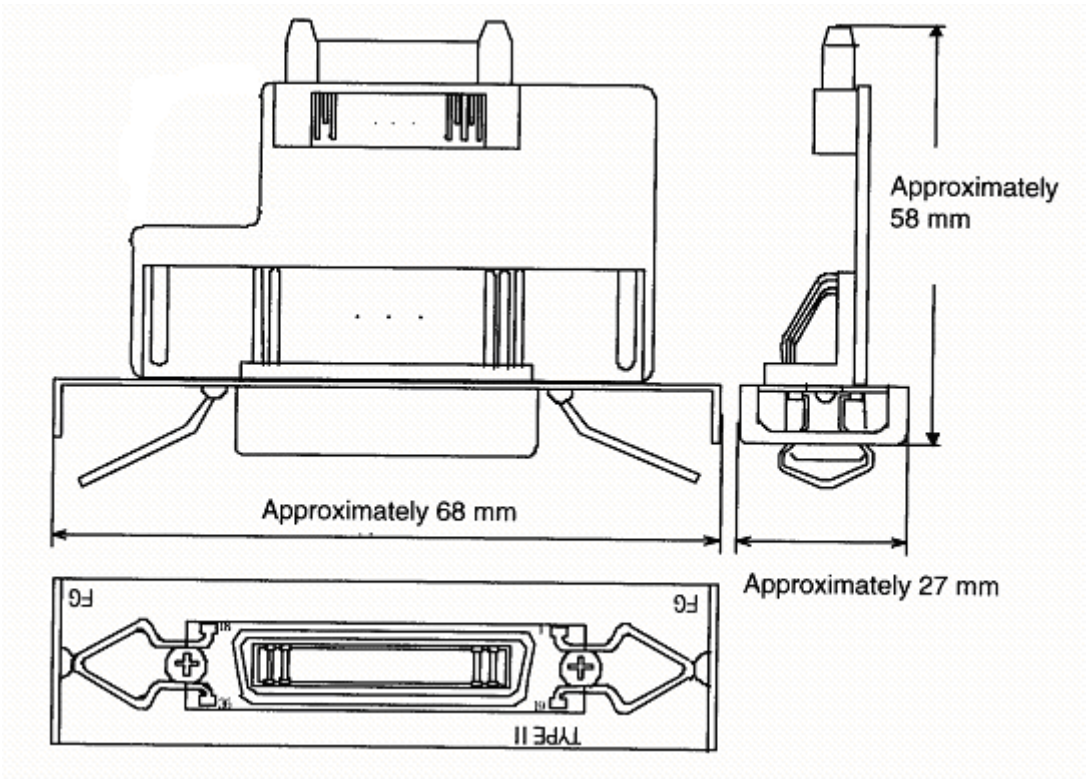


Figure 3.2.1 External View of the Parallel Interface Board

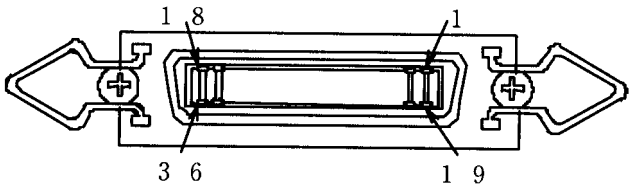


Figure 3.2.2 External Font View of Parallel Interface Connector

*The connector used on this interface board is equivalent to a 1284 Type B.

4. EMC APPLIED

EMC is tested using the EPSON TM series printers with the optional power supply provided by EPSON.

1) Europe: CE marking
Directive 2004/108/EC
EN55022 Class B
EN55024
IEC61000-4-2
IEC61000-4-3
IEC61000-4-4
IEC61000-4-5
IEC61000-4-6
IEC61000-4-11

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3) Japan: EMI VCCI Class A
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4) Oceania: EMI AS/NZS/CISPR22 Class B